IN THE CLAIMS:

Please amend claims 2, 3 and 6 as follows:

1. (Previously Presented) A method for storing data, said method comprising the steps of:

generating a glitchless fractional clock pulse in a circuit, wherein said glitchless fractional clock pulse is of a shorter period than a system core clock pulse;

transmitting the glitchless fractional clock pulse from the circuit to a data storage element; and

storing data in the storage element upon receiving the glitchless fractional clock pulse.

2. (Currently Amended) A method for storing data, said method comprising the steps of:

generating a glitchless fractional clock pulse in a circuit;

transmitting the glitchless fractional clock pulse from the circuit to a data storage element; and

storing data in the storage element upon receiving the glitchless fractional clock pulse, wherein said step of generating a glitchless fractional clock pulse further comprises the steps of:

receiving a data ~~storage enable~~ signal at a first input to the circuit;

receiving a system clock signal at a second input to the circuit;

generating the glitchless fractional clock pulse in the circuit, wherein a period of the glitchless fractional clock pulse is less than a period of the system clock signal; and

outputting the glitchless fractional clock pulse at an output of the circuit.

3. (Currently Amended) A method for storing data as recited in claim 2, wherein said step of

generating the glitchless fractional clock pulse further comprises the steps of:

transmitting the data ~~storage enable~~ signal to a first flip-flop;

transmitting the system clock signal to the first flip-flop and a second flip-flop;

receiving an output of the first flip-flop at a first input of an AND gate and the second flip-flop;

receiving an output of the second flip-flop at a second inverted input of the AND gate; and

generating the glitchless fractional clock pulse at an output of the AND gate.

4. (Original) A method for storing data as recited in claim 3, wherein the glitchless fractional clock pulse generated on the output of the AND gate is transmitted to an enabling input of the data storage element.

5. (Previously Presented) A method for storing data, said method comprising the steps of:

generating a glitchless fractional clock pulse in a circuit;

transmitting the glitchless fractional clock pulse from the circuit to a data storage element; and

storing data in the storage element upon receiving the glitchless fractional clock pulse, wherein the data storage element further comprises at least one latch.

6. (Currently Amended) A method for storing data, said method comprising the steps of:

generating a glitchless fractional clock pulse in a circuit;

transmitting the glitchless fractional clock pulse from the circuit to a data storage element; and

storing data in the storage element upon receiving the glitchless fractional clock pulse, wherein the step of generating the glitchless fractional clock pulse further comprises the steps of:

receiving a clock signal at a first input to the circuit, the clock signal having a plurality of equally spaced and timed pulses, each of the pulses having a rising edge and a falling edge;

receiving a data ~~storage enable~~ signal at a second input to the circuit; and

generating the glitchless fractional clock pulse on an output of the circuit in response to the data storage enable signal, wherein a duration of the glitchless fractional

clock pulse is less than a duration of the clock signal pulse and is positioned between the rising edge and falling edge of a corresponding clock pulse.

7. (Original) A method for storing data as recited in claim 6, wherein said transmitting step further step further comprises transmitting the glitchless fractional clock pulse from the output of the circuit to the storage element

8. (Previously Presented) A method for storing data, said method comprising the steps of:

generating a glitchless fractional clock pulse in a circuit;

transmitting the glitchless fractional clock pulse from the circuit to a data storage element; and

storing data in the storage element upon receiving the glitchless fractional clock pulse, wherein the step of generating a glitchless fractional clock pulse further comprises generating a glitchless fractional clock pulse having a period less than a period of a system core clock pulse.

9. (Previously Presented) A method for storing data, said method comprising the steps of:

generating a glitchless fractional clock pulse in a circuit;

transmitting the glitchless fractional clock pulse from the circuit to a data storage element; and

storing data in the storage element upon receiving the glitchless fractional clock pulse, wherein the step of generating the glitchless fractional clock pulse further comprises generating the glitchless fractional clock pulse, wherein the glitchless fractional clock pulse is generated between a rising edge and a falling edge of a system core clock pulse.

10. (Previously Presented) A method for enabling a latch, said method comprising the steps of:

receiving a clock signal in a logic circuit;

receiving a latch enable pulse in the logic circuit;

generating a glitchless fractional clock pulse in the logic circuit in response to the latch enable pulse and the clock signal, wherein said glitchless fractional clock pulse is of a shorter period than a system core clock pulse; and

transmitting the glitchless fractional clock pulse to a gate input of a latch to enable the latch to store data during an optimally stable time period.

11. (Previously Presented) A method for enabling a latch, said method comprising the steps of:

receiving a clock signal in a logic circuit;

receiving a latch enable pulse in the logic circuit;

generating a glitchless fractional clock pulse in the logic circuit in response to the latch enable pulse and the clock signal; and

transmitting the glitchless fractional clock pulse to a gate input of a latch to enable the latch to store data during an optimally stable time period, wherein the step of generating a glitchless fractional clock pulse further comprises the steps of:

receiving the latch enable signal at a first input of a first flip flop;

receiving the clock signal a second input of a second flip-flop and at a second input of the first flip-flop;

receiving an output of the first flip-flop at a first input of the second flip-flop and a first input of an AND gate;

receiving an output of the second flip-flop at a second inverted input of the AND gate; and

generating the glitchless fractional clock pulse at an output of the AND gate.

12. (Original) The method for enabling a latch as recited in claim 11, wherein the step of transmitting the glitchless fractional clock pulse further comprises transmitting the glitchless fractional clock pulse from the output of the AND gate to the gate input of the latch.

13. (Previously Presented) An apparatus for storing data, said apparatus comprising:

at least one storage element having a data input, a storage enable input, and a data output; and

at least one logic circuit having an activating input, an clock input, and a logic output,

wherein the at least one logic circuit generates a glitchless fractional clock pulse on the logic output, said logic output being connected to the storage enable input of the storage element and operating to enable the at least one storage element to store data resident on the data input at an optimally stable time, and wherein said glitchless fractional clock pulse is of a shorter period than a system core clock pulse.

14. (Original) An apparatus for storing data as recited in claim 13, wherein the at least one storage element further comprises at least one latch.

15. (Previously Presented) An apparatus for storing data, said apparatus comprising:

at least one storage element having a data input, a storage enable input, and a data output; and

at least one logic circuit having an activating input, an clock input, and a logic output,

wherein the at least one logic circuit generates a glitchless fractional clock pulse on the logic output, said logic output being connected to the storage enable input of the storage element and operating to enable the at least one storage element to store data resident on the data input at an optimally stable time, wherein the at least one logic circuit further comprises:

a first flip flop having a first CLK input, a first data input, and a first output;

a second flip flop having a second CLK input, a second data input, and a second output; and

an AND gate having a first input, a second inverted input, and an output,

wherein the first output of the first flip flop is connected to the second data input of the second flip flop and the first input of the AND gate, the second output of the second flip flop is connected to the second inverted input of the AND gate, a system clock pulse is connected to the first CLK input and the second CLK input of the first and second flip flops, a latch enable pulse is received on the first data input of the first flip flop, and a glitchless fractional clock pulse is generated on the output of the AND gate and transmitted to the storage enable input on the storage element.

16. (Previously Presented) An apparatus for storing data, said apparatus comprising:

at least one storage element having a data input, a storage enable input, and a data output; and

at least one logic circuit having an activating input, an clock input, and a logic output,

wherein the at least one logic circuit generates a glitchless fractional clock pulse on the logic output, said logic output being connected to the storage enable input of the storage element and operating to enable the at least one storage element to store data resident on the data input at an optimally stable time, wherein the glitchless fractional clock pulse generated at the logic output of the AND gate further comprises a glitchless fractional clock pulse having a width that is less than a width of a system clock pulse and positioned between a rising edge and a falling edge of the system clock pulse.

17. (Previously Presented) A network switch for switching data, said network switch comprising:

at least one data port interface;

at least one storage element in connection with the at least one data port interface and having a data input, a storage enable input, and a data output; and

at least one logic circuit having an activating input, a clock input, and a logic output,

wherein the at least one logic circuit is configured to generate a glitchless fractional clock pulse on the logic output, said logic output being connected to the storage enable input of the storage element and operating to enable the at least one storage

element to store data resident on the data input at an optimally stable time, and wherein said glitchless fractional clock pulse is of a shorter period than a system core clock pulse.

18. (Previously Presented) A network switch for switching data, said network switch comprising:

at least one data port interface;

at least one storage element in connection with the at least one data port interface and having a data input, a storage enable input, and a data output; and

at least one logic circuit having an activating input, a clock input, and a logic output,

wherein the at least one logic circuit is configured to generate a glitchless fractional clock pulse on the logic output, said logic output being connected to the storage enable input of the storage element and operating to enable the at least one storage element to store data resident on the data input at an optimally stable time, wherein said network switch further comprises a communication channel in connection with the at least one data port interface for communicating data in the network switch.

19. (Original) A network switch as recited in claim 17, wherein said network switch further comprises a memory management unit for controlling the storage of data in the at least one storage unit.

20. (Previously Presented) An apparatus for storing data, said apparatus comprising:

a storage means for storing data, said storage means having an input for receiving data to be stored, a storage enable input for enabling the storage means, and a data output; and

at least one pulse generating means for generating a glitchless fractional clock pulse, said pulse generating means having an activating input, a clock input, and an output in connection with the storage enable input of the storage means,

wherein the pulse generating means generates the glitchless fractional clock pulse that is transmitted to the storage means to enable the storage means to store data at an optimally stable time, and wherein said glitchless fractional clock pulse is of a shorter period than a system core clock pulse.

21. (Original) An apparatus for storing data as recited in claim 20, wherein said storage means further comprises at least one latch.

22. (Previously Presented) An apparatus for storing data, said apparatus comprising:

a storage means for storing data, said storage means having an input for receiving data to be stored, a storage enable input for enabling the storage means, and a data output; and

at least one pulse generating means for generating a glitchless fractional clock pulse, said pulse generating means having an activating input, a clock input, and an output in connection with the storage enable input of the storage means,

wherein the pulse generating means generates the glitchless fractional clock pulse that is transmitted to the storage means to enable the storage means to store data at an optimally stable time, wherein said pulse generating means further comprises:

a first flip flop having a first CLK input, a circuit enable input, and a first output;

a second flip flop having a second CLK input in connection with the first CLK input of the first flip flop, a data input in connection with the first output of the first flip flop, and a second output; and

an AND gate having a first input in connection with the first output of the first flip flop, a second inverted input in connection with the second output of the second flip flop, and an output,

wherein the glitchless fractional clock pulse is generated on the output of the AND gate upon receiving an enable pulse at the circuit enable input.